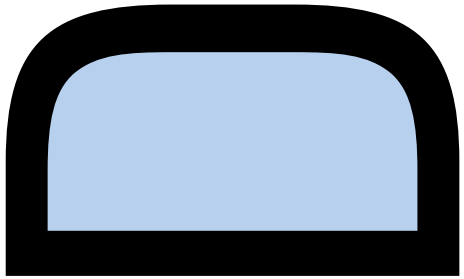
WHITE PAPER SERIES / EDITION 1



AUTO–ID LABS

BUSINESS PROCESSES & APPLICATIONS
SOFTWARE & NETWORK
HARDWARE

AUTOIDLABS-WP-HARDWARE-012

An HF/UHF RFID Analogue Front-end Design and Analysis

Zheng Zhu, Behnam Jamali, Peter H. Cole

School of Electrical and Electronics Engineering,
The University of Adelaide, SA 5005, Australia

{zzhu, bjamali, cole}@eleceng.adelaide.edu.au
www.autoidlabs.org

AUTO-ID LABS

This paper describes a passive HF/UHF RFID tag chip front-end design and the preliminary test results, including different rectifier structures, regulator and protector, demodulator and modulator, power on reset, etc. The paper also analyses the possible cause of the discrepancies between the designed Schottky diode and the other people's work. Based on the test results and analysis, the paper points out the future work to do on the passive RFID tag chip front-end design.

1. Background

One of the main objectives of the Auto-ID Lab Adelaide is the mastery of RFID tag chip design in up to date technologies. This research project of "passive RFID tag chip design" deals with the challenges of low supply voltage, ultra low power consumption large input power dynamic range, weak back scattering, and efficient antenna matching. Among all the RFID tag chip circuit blocks, a high sensitivity and efficient rectifier is probably the hardest to achieve. It is proposed to carry more research on Schottky diode in standard CMOS technology as well as to develop critical frontend detector circuits for high performance tag. According to the schedule, a prototype chip of UHF RFID tag chip frontend was designed from July to October, 2004 and taped out at the end of October, 2004. This paper will introduce the design of the RFID front-end, preliminary testing results and analysis, and the future work. We will introduce the chip design in section 2 and Schottky diode design in section 3. The testing results will be listed in section 4. In section 5, we will analyse the possible cause of discrepancy and we will give summary and future work in section 6.

2. Chip Design

The major blocks and their functions of the RFID front-end are:

- ***Rectifier:*** to generate the power supply voltage for front-end circuits and the whole chip as well from the coupled EM field
- ***Power (voltage) regulator (protector):*** to maintain the power supply at a certain level and at the same time prevent the cir cuit from malfunctioning or breaking under large input RF power

- ***Demodulator:*** to extract out the data symbols which are embedded in the carrier waveforms
- ***Clock extraction or generation:*** to extract the clock out of carrier (usually in HF systems) or generate the system clock by some kinds of oscillators
- ***Back-scattering:*** to fulfil the return link by alternating the impedance of the chip
- ***Power on Reset:*** to generate the chip power on reset (POR) signal
- ***Voltage (current) reference:*** to generate some voltage or current reference for the use of front-end and other circuit blocks, usually in the term of band-gap reference
- ***Other circuits:*** like the persistent node or short-term memory, ESD, etc.

Figure 1 is the block diagram of a typical RFID front-end.

As the most important part, we designed several different rectifier structures for the prototype chip. Not only embedded (as a part of the front-end) but also the stand-alone rectifiers are designed. We found that the PMOS rectifier has overall good performance at nominal input voltage level (4Vth, i.e.). [1] So we designed two sets of PMOS rectifiers to verify the efficiency. If the maximum input voltage level decreases to a little bit than 2Vth, we have to use the PMOS and NMOS gate cross-connected bridge rectifier[i]. We also have two different stand-alone rectifiers for test and verification. Only the Schottky diode (or other low turn-on voltage diodes) voltage doubler can work under the input voltage level around 1 or 2 threshold voltage. In order to test the output DC voltage versus diode dimensions, we designed two different test blocks. One has 10 stages; the diode has minimum contact area and perimeter, (AD=0.23p, PJ=1.92u). The stage store capacitor value is 237f. And the other has 10 stages, too. While the diode area is in the middle range, (AD=1.4976p, PJ=7.2u). The capacitor values are the same.

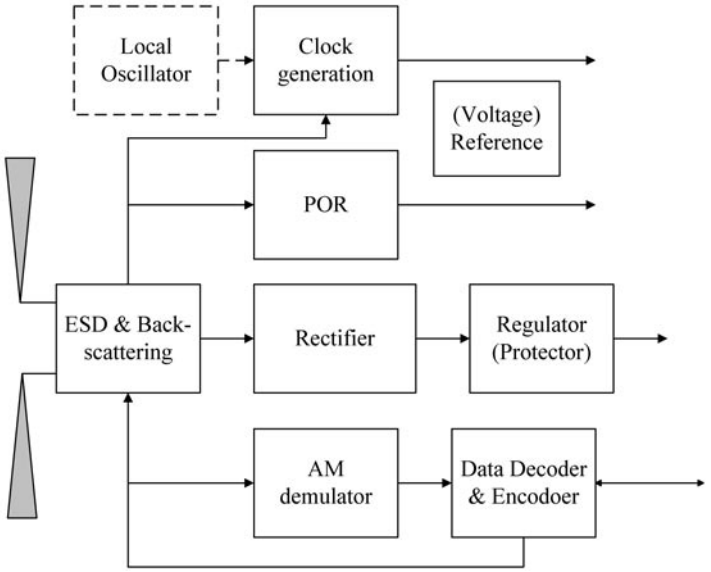


Fig. 1: RFID front-end block diagram

The regulator (protector) has two major functions. One is to regulate the front-end output supply voltage level to a preferred value and within a preferred range. For example, output voltage to the digital core is 2.5V. The other is to protect the inner circuits from breaking at high RF input power levels. As we know, The EM field strength may vary in the magnitude of tens even hundreds of times at different physical locations. If all the conditions remain the same, the RF input power to the tag chip can vary in the same magnitude of the EM field strength. There must be circuits inside the analogue front-end to overcome the variation. Because of the fact that the EM field variation is huge, a single circuit block usually cannot handle the situation. We usually use different sub

circuit blocks to carrier the protection and regulation functions separately. Nevertheless, the circuit structures are similar. There are two basic approaches to fulfil the regulation/protection. One is the shunt regulation and the other is coupling factor attenuation.

As we know, for a fixed input electric power, the higher the current, the lower the voltage. So what the shunt regulator does is to bypass the surplus power to some shunt routes so as to keep the output voltage unchanged. Although there might be a lot of implementations of the shunt regulation circuits, the basic ideas of the shunt regulation are the same. The shunt regulator is a kind of negative feedback system. The value we have to control is voltage, so we have to use some voltage reference as the control input. And the voltage difference between the reference and the input (or ratio of the input) is fed into or magnified then fed into some kind of voltage controlled variable resistors so as to change the overall output current and suppress the output voltage variations. Figure 2 is the shunt regulator design used in the frontend chip. The circuit block uses ratio of the output voltage to control the Vgs of a MOS transistor M3, which is working in the saturation region. This MOS transistor serves as the variable load. By varying the current of the MOS transistor M3, the overall load current of the rectifier output will be changed. The current of M3 is given by (assuming that $V(D) = V(A) - V_{gs1} - V_{gs2} - V_{gs4} - V_{gs5} \approx V(A) - 4V_{gs1}$:

$$I(M_3) = \frac{1}{2}\beta_{M3}[V(A) - 4V_{th} - \frac{3}{k}\sqrt{k[V(A) - 4V_{th}] + 4} + \frac{6}{k}]^2, \quad k = \frac{1}{2}\beta_{M1} \cdot R_1 \quad (1)$$

We can choose the transistor parameters according to the system specification by equation 1. We start from the input RF power dynamic range. The RF power dynamic range is usually given by the regulation and the chip power consumption estimation. The minimum chip power consumption is the index of the maximum operation distance that the tag can work at. And the regulation forms maximum RF input power. For the HF case, we can convert the maximum magnetic field to the form of maximum input power. For the UHF case, with the maximum ERP about 500mW and antenna gains of 0dB, we can estimate the maximum input power to the tag is around 60mW for a distance of 10 cm. The dynamic range of the UHF range input power is around 100mW to 200mW.

With the input power dynamic range as well as the tolerable voltage variation of node A, we can get the maximum current of M3 so does the β_{M3} and k.

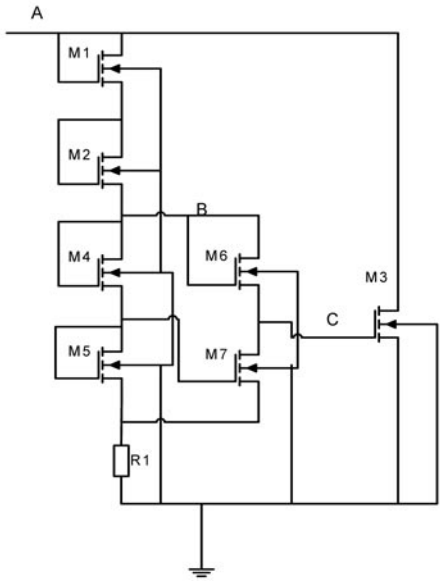


Fig. 2: Shunt regulator schematic

Demodulator is another key circuit block inside the analogue front end. Although the modulation schemes to use in the reader might be different, some of them are amplitude modulation, and some of them are phase modulation. What the analogue front-end demodulator can demodulate is only in the form of amplitude change or "dip". So the demodulator is actually an edge detector. The figure 3 is the envelope detector and the AM demodulator (comparator) we designed. After the input carrier waveform is passed through the envelope detector, a low-pass filter is used to filter out the carrier ripple noise residue. Then the signal and its low pass filtered one is fed into a hysteresis comparator to generate the output.

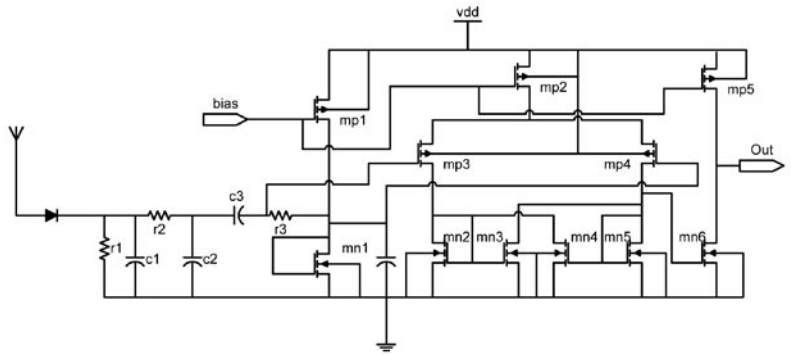


Fig. 3: Envelop detector and AM demodulator

As a counterpart of the demodulator, the backward link modulator is another essential part of the RFID analogue frontend. In the analysis of the RFID systems it is important to consider whether the labels are placed in the far (propagating) or near (energy storage) fields of the reader (interrogator) antenna. Usually, the working ranges of the HF and UHF RFID systems are different. The HF RFID systems are based on magnetic coupling of magnetic systems. The magnetic coupled communication is only possible if the near field condition: $d < \lambda/(2\pi)$ is valid [2].

By this criterion, we can see that the UHF RFID systems are working in the far field. Since the working ranges are different, the coupling operations as well as the backward modulation algorithms are different. The UHF RFID backward link mechanism is the reflection co efficiency modulation (by alternating the radar cross section of the tag). We found that the communication bottlenecks still exist on the tag power consumption by numeric analysis. At 4-meter distance, the maximum input power to the tag IC is only 64uW with the antenna gain 1.64 (or 39uW with the antenna gain of odB). Considering the rectifier efficiency at low input power, it is really a challenge for the chip designer. The backward power at the reader receiver end is around–75dBm to –61dBm by our calculation. However, we need about –90dBm to implement the "listen before talk" to meet the EM regulations. So the backward signal power is not a bottleneck for the tag chip design.

Since the impedance is a vector, we might be able to get the wanted $\Delta RCS_{1,2}$ by only varying the real or imaginary part or both of them. The paper [3] gives a detailed analysis over the back modulation and power supply efficiency issues. It is recommended to put the tag IC impedance to two states with same real parts but symmetrical imaginary parts in this paper. And it is called as PSK with an equal amount of mismatch in both states. We also learn that the power efficiency to the tag IC is also affected by the ratio of the reflected back power besides the modulation method. By our analysis, we have found that 10% or so of the reflection ratio is enough for the reader receiver. The modulation of the imaginary part of the tag IC impedance is easier to achieve by modulation of the capacitance rather than inductance in silicon implementation. We used the same circuit structure as in the paper [3]. The digital core has to have the system clock to run the state machine or mi-

croprocessor and decode and encode the data. So every RFID tag chip needs a clock generation circuit block and the clock generation is always a part of the RFID front-end. For the HF (13.56MHz) system, it is easy to extract the clock signals from the carrier and divide down to feed into the digital core. We can use a simple invertor to fulfil the work. Comes to the UHF systems, we cannot use the direct extracting approach. The carrier frequency is tens of thousand times higher than the data rate; it is unrealistic to directly divide the carrier down for the digital core because of the complication and huge power consumption. We have to implement an on chip oscillator to generate the system clock in UHF tag chips (Some of the communication protocols provide embedded clock in the carrier waveform so a separate clock generation is not needed). The clock generated by on chip oscillator has two major usages: one is the state machine (digital core) clock, which does not have to have a specific frequency as long as the processing speed is enough to meet the turn around time and the power budget; the other is the decoding and encoding of the data. If we want a specific frequency, we need a feedback loop structure, such as PLL, to tune the local oscillator. And this will increase the chip cost and the power consumption. So the protocols usually have relative timing rather than absolute timing values. For example, EPC C1G2 protocol uses PIE (pulse interval encoding) for the reader to tag link and FMo or Miller encoded sub-carrier for the tag to reader link. The PIE itself is relatively timed. As long as the local oscillator frequency is higher than the highest symbol rate (1/Tari(min)), the decoder can easily decode the PIE encoded data out. And for the backward modulation, the link frequency is also a kind of time range rather than a few fixed values. So a simple local oscillator maybe enough to fulfil the task as long as the output frequency can remain stable within the spec. We designed a five stage simple oscillator in the prototype chip. The figure 4 is the schematic of the oscillator.

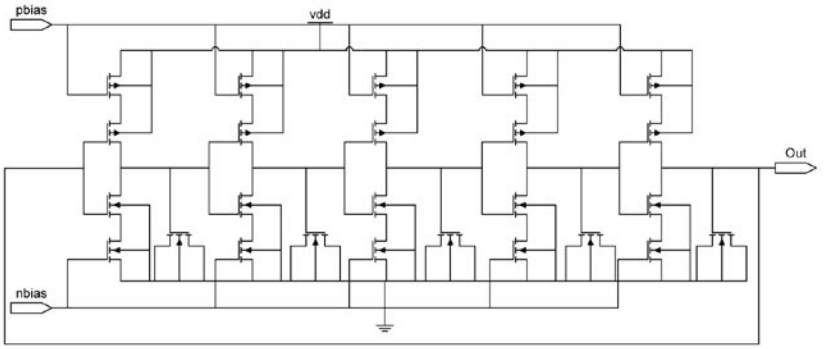


Fig. 4: Local oscillator

We use the bias generation to control the oscillator stage charge and sink current, which is directly proportional to the clock period. However, the structure cannot control the node voltage swing so as to control the output frequency. The output frequency is reverse proportional with the supply voltage. The output frequency goes down with the increase of the power supply. However, the power supply is regulated within a certain range by regulators.

Besides the circuit blocks already described, there are some other circuit blocks designed in the prototype chip. The detailed description will not be given in the paper considering the length of the paper.

3. Schottky Diode Desig

Only the voltage doubler (multiplier) structure rectifier with low turn on voltage devices such as Schottky diode can achieve optimal efficiency at low input levels [1]. The CMOS compatible

Schottky diode is also designed in the prototype chip. Schottky diodes have been widely used in microwave networks for many years because of their excellent high frequency behaviour [4][5][6][7][8]. The properties of forward-biased Schottky barrier diodes are determined by majority carrier phenomena, while those properties for p-n diodes are primarily determined by minority carriers. The result of this is that the Schottky diodes can be switched faster. And the built in barrier height of the Schottky barrier diodes are usually lower than the p-n junction diodes. The results of this is that the Schottky diodes can be turned on at lower forward bias voltage which makes them a excellent candidate for low input level rectifier applications. For microwave applications, these Schottky diodes are usually fabricated in specialized processes where barrier heights, capacitances and other parameters can be fully controlled [4]. However, the RFID application demand low cost solution and pushes using the standard CMOS processes. Several research works have been published on standard CMOS processes compatible Schottky diodes [4][9][10][11]. The Schottky diode structure we use is similar to the works in [10] and [11].

The rectifying properties of Schottky contacts are determined by the work function of the majority carriers, as Schottky originally called the barrier height. This quantity equals the distance in energy between Fermi level and the edge of the respective majority carrier band [12]. The built-in potential of the metal-semiconductor junction, ϕ_i, is defined as the difference between the Fermi energy of the metal and that of the semiconductor.

$$\phi_i = \Phi_M - \chi - \frac{E_c - E_{F,n}}{q}, n-type \qquad (2)$$

$$\phi_i = \chi + \frac{E_c - E_{F,p}}{q} - \Phi_M, p-type \qquad (3)$$

To form a rectifying junction for an n-type semiconductor, the work function of the metal Φ_M, should be larger than the n-type semiconductor Fermi level. And for a p-type semiconductor, it requires that the work function of the metal Φ_M, must be smaller than the p-type semiconductor Fermi level which is close to the valence band (sum of the electron affinity and the band-gap energy). Since the typical electron affinity is about 4eV (4.05eV for silicon) and forbidden band gap value is 1.115 eV for silicon, and the lightly doped p-type semiconductor we can use in the proposed process is p-substrate whose Fermi level might be too close or even smaller than the work function Φ_M, of contact metal, tungsten. We only designed metal to n-type semiconductor Schottky contact in the prototype chip. We are trying to form Schottky contact by directly deposition of the contact metal, tungsten, over lightly doped N-well semiconductor. Since the process is fixed, what we can control is only the geometry of the Schottky contact. We designed several different Schottky diodes as listed in table 1.

Schottky Diode Name	Junction Area	Junction Peri	Finger Number	W*L
SBD1	0.23p	1.92u	1	0.48um*0.48um
SBD2	0.23p	1.92u	1	0.48um*0.48umi
SBD3	1.4976p	7.2u	1	0.48um*3.12um
SBD4	16.128p	72.9u	6	0.48um*5.6um
SBD5	14.4p	60.96u	1	0.48um*30umii

Table 1: Schottky barrier diodes geometry description

[i] The SD1 and SD2 have same junction area. The SD1 anode and cathode are connected by metal1 while the anode of SD2 is connected out by metal2 so as to make the cathode contacts surround the junction as a circle (donut shape).

[ii] Extra-long junction dimension Schottky Diode is fabricated to verify our understanding over the dimension effects.

4. Preliminary Test Results

The prototype chip uses Shanghai Huahong-NEC CZ6H double poly triple metal CMOS 0.35um process with embedded EEPROM. The prototype chip samples were fabricated and packaged at the end of January 2005. With the supports from Auto-ID lab @ Fudan University, we got some preliminary test results on the Schottky barrier diode and the frontend interface as well. The preliminary test results are given in this section and more testing and discoveries will be documented later on.

The DC characteristics of the Schottky diodes are plotted in figure 5. The turn on voltage from the measurement is more than 0.8V by intercept the current curves at linear range. While the reverse break down voltages are not bad which are more than -10V.

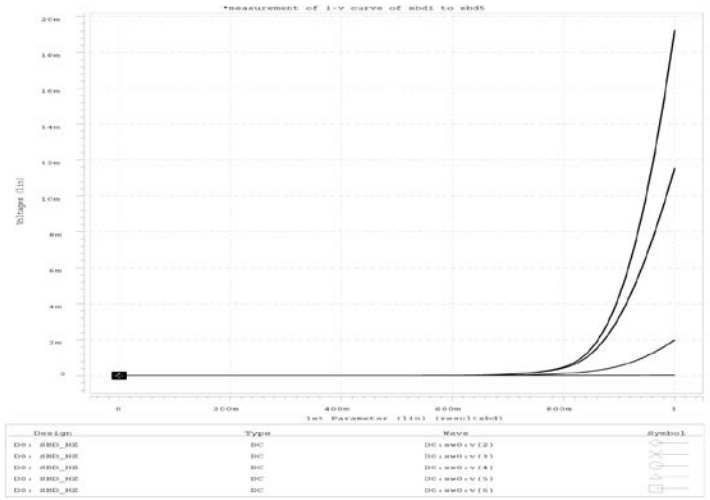


Fig. 5: Measured I-V curves of Schottky diodes

Considering the series resistor and if the bias voltage is larger than 3Vt, the I-V function of the Schottky diode can be expressed as:

$$I = I_s \exp(\frac{V - IR_s}{nV_t}) \qquad (4)$$

And the Schottky barrier height B + can be expressed as:

$$\phi_B = V_t \cdot \ln(\frac{A \cdot A^* \cdot T^2}{I_s}) \qquad (5)$$

Using the measured I-V curve data, we get the parameter of the Schottky barrier diodes as listed in table 2: (The SBD1 and SBD2 have a very large series resistance, more than a few hundreds ohm by regression of the measured data and not listed in the table.)

	Junction Area	Finger number	Rs (ohm)	Is (A)	ϕ_B (by equation 5) (eV)
SBD3	1.4976p	1	69	4.66E-11	5.61E-01
SBD4	16.128p	6	6.7	4.08E-11	6.26E-01
SBD5	14.4p	1	12	6.12E-11	6.12E-01

Table 2 Schottky barrier diodes parameters

The barrier heights of the Schottky diodes are comparatively higher than the results in [10] but smaller than the results in [4]. The relatively high barrier height results poor rectify efficiency because of the high resistance of the diode. This parameter cannot be controlled by fabrication through the commercial CMOS foundry [4]. Since the doping concentration of the N-well is not available from the foundry until now, we are not able to extract the barrier potential from the C-V measurement results to verify the results calculated by equation 5.

We measured the regulator characteristics. The regulator consists of two parts as we know, one is the protection shunt regulator and the other is a parallel structure regulator. The regulator

will not regulate the output voltage until the input power supply reaches around 2V. And the shunt regulator will protect the inner circuit by shunting oversupplied current when the input supply voltage reaches above 5.4V or so. The shunted power is 130mW at input supply if 6.5V and 315mW at input supply of 6.8V. The regulator output voltage (VDD) remains between 2V to 2.45V at the input power level between 60uW to 350mW.

Thanks to the regulation of the power supply, the on-chip oscillator's output clock varies less than +/- 10% of the designed value. Table 3 lists the output frequency of the oscillator versus the input power level of the regulator.

Regulator input level (VCC) (Volt)	1.8	2.0	2.5	2.7	3.0	3.5	3.9	5
Output frequency (KHz)	127	137	137	135	133	129	125	120

Table 3: On-chip oscillator measurement results

The input impedance of the rectifiers and the interface circuits are under test. So the efficiency comparison of the rectifiers, demodulator, back scattering, etc. haven't done yet. The results will be documented in future.

5. Analysis

Since we only measure the I-V curves between anode (contact metal directly over N-well) and cathode (N-well), we are sure the diode characteristics are the Schottky diodes' rather than some other parasitic diodes. What is the main cause of the larger barrier height of our design? The comparatively higher barrier height and the turn on voltage of the Schottky barrier diodes is determined by the process we use. The tungsten work function in vacuum is about 4.6eV and the barrier height measured of tungsten and n-type silicon barrier height is 0.67eV [13]. The data are actually very close to the one we got. The Schottky barrier is formed by contact metal (Tungsten in the process we used) and the lightly doped semiconductor (N-well we chose). The metal property, doping concentration of the N-well and the interface states determine the barrier height. As we know, if we increase the doping concentration of N-well, the Schottky contact will finally become an ohmic contact (tunnelling effects). If we would be able to get the N-well doping concentration, we will be able to use measured C-V data and function 6 to correlate the barrier height.

$$C_j = A \cdot \sqrt{\frac{q \cdot \varepsilon_s \cdot N_d}{2 \cdot (\phi_i - V_a)}} \qquad (6)$$

Another consideration is whether we missed any process steps to form a good metal-semiconductor contact. After we double-checked the process steps and discussed with some other people, we found that a mask named filed (by adding N+ and P+ together) will be generated in the process we used for the prototype this time. Usually, we call this mask "active". Some of the processes use this mask to mask out the oxidation formation before the contact metal deposition. If the contact hole is not protected by photoresist, it is possible that the contact etching is not clean enough and there will be residue of the oxide particles exist between the contact metal and the semiconductor. And these process steps are performed just before the contact metal formation. And we checked the foundry manual, and we found that the mask "filed" is used during the first a few process steps and has no much relationship with the contact formation. So we think we didn't miss

any process steps, which will affect the formation of metal-semiconductor contact.

The measurement shows that the series resistance is very high. Only when the contact area is over 10p m^2, the series resistance comes down to the range of tens ohm. The high series resistor plus the lower saturation current makes the turn-on voltage of the Schottky diodes not as attractive as we expected.

6. Summary

We designed and fabricated an UHF/HF RFID tag chip RF interface and some other important built-in blocks as well. The preliminary results demonstrated that the Schottky barrier height formed by contact metal tungsten and lightly doped N-type silicon is around 0.6eV and the turn-on voltage of the Schottky diodes are over 0.8V. These characteristics are determined by the process we use and make the diodes not attractive to use in the ultra-low input level as we analysed [1]. The difference between the characteristics of the Schottky diodes [4, 10] and our work demonstrates that RFID friendly CMOS compatible Schottky diodes are not an easy on-shot task. If the extra process steps are not available, every possible approach should be tried and tested. For example, the contact metal and P-type silicon, contact metal and slightly high doped N-type silicon, round contact shape, etc. These possible approaches will be designed and tested in future.

Part of the RF interface functions are also tested and verified. In future, we will measure the input impedance of the RF interface and discrete rectifiers. Then impedance matching networks will be designed and the efficiency of the rectifiers will be tested and documented.

AUTO-ID LABS

References

[1] Zheng Zhu, etc. “Brief Comparison of Different Rectifier Structures for RFID Transponders”, Auto-ID labs workshop, St Gallen, Switzerland, Sept. 2004.

[2] Klaus Finkenzelle, RFID Handbook, Hanser Verlag, Germany.

[3] Udo Karthaus, Martin Fischer, “Fully Integrated Passive UHF RFID Transponder IC with 16.7uW Minimum RF Input Power”, IEEE Journal of Solid-State Circuits, Vol. 38, No. 10, Oct. 2003.

[4] Veljko Milanovic, etc. “CMOS Foundry Implementation of Schottky Diodes for RF Detection”, IEEE Transactions on Electron Devices, Vol. 43, No.12, December 1996.

[5] B.L. Sharma, Metal-Semiconductor Schottky Barrier Junctions and Their Applications. New York: Plenum, 1984.

[6] R.E. Lafferty, “Diode sensors for the measurement of true power”, Microwave J., pp. 46-49, Nov. 1987.

[7] S. Mollenkopf and G. M. Rebeiz, “A 22 GHz MIC active receiriver/radiometer”, IEEE MTT-S Int. Microwave Symp. Dig., Vol. 3, pp. 1347-1350, May 1994.

[8] K. M. Strohm, etc. “Millimeter wave transmitter and receiver circuits on high resistivity silicon”, IEE Coll. On Microwave and Millimeter Wave MIC, Nov. 1988, No. 17, pp. 1-4.

[9] Karl M. Strohm, etc. “SIMMWIC Rectennas on High-Resisivity Silicon and CMOS Compatibility”, IEEE Transactions on Microwave Theory and Techniques, Vol. 46, No. 5, May 1998

[10] Qiang Li, etc. “Fabrication and Modelling of Schottky Diode Integrated in Standard CMOS Process”, Auto-ID labs workshop, St Gallen, Switzerland, Sept. 2004.

[11] Behnam Jamali, etc. “Desing and optimisation of Schottky diodes in CMOS technology with application to passive RFID systems”, Proc. SPIE, Smart Structures, Devices, and Systems II, Vol. 5649, p. 323-331, Dec. 2004

[12] Winfried Mönch, Electronic Properties of Semiconductor Interfaces, Springer-Verlag Berlin Heidelberg, 2004, pp. 4

[13] http://www.mtmi.vu.lt/pfk/funkc_dariniai/diod/schottky.htm#(1)