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A Low Voltage Low Power RF/Analog Front-end Circuit for Passive UHF RFID Tag

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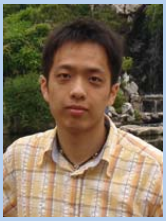

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Abstract

This paper presents a low voltage low power RF/analog front-end circuit for passive ultra high frequency (UHF) radio frequency identification (RFID) tag. Temperature compensation is achieved by a reference generator using sub-threshold techniques which requires lower supply voltage than conventional bandgap circuit. Some novel structures are developed to construct the building blocks, including a zero static current power-on reset circuit and a voltage regulator. The RF/analog front-end circuit is implemented with digital base-band and EEPROM in 0.18 μm CMOS EEPROM technology. Measurement results show that the tag has a minimum supply voltage requirement of only 0.75 V.

1. Introduction

Cheap and adaptable, passive radio frequency identification (RFID) tags operating in ultra high frequency (UHF) band are showing a wide prospect of applications. Nowadays, technology trend for passive UHF tags is to increase the operating distance, reading rate and reading speed. Therefore, stringent requirements are proposed, including low power, high power conversion efficiency (PCE) and stability against different working conditions. In recent years, various optimizations have been introduced to enhance the tag's performances [1]-[4]. However, most of them used the CMOS technology with Schottcky diodes which is relatively expensive. Moreover, few work mentions the realization of temperature compensation, without which the tag can not work correctly in a large temperature span.

We designed a whole tag chip in CMOS technology with EEPROM. The RF/analog front-end circuit distinguishes itself by its adaptability to standard CMOS technology, a low power characteristic (especially a supply voltage requirement of only 0.75 V), and a temperature insensitivity performance.

The organization of the paper is as follows. In Section 2, the system architecture and low voltage considerations are presented. In Section 3, we analyze the concept of impedance matching. In Section 4, building block design is described in detail. In Section 5, simulation and measurement results are illustrated. And finally, we draw a conclusion in Section 6.

2. Circuit Architecture

Fig. 1 depicts the architecture of our tag, where the circuit in the dotted line frame represents the RF/analog front-end. The circuit derives its power supply by rectifying the interrogating RF energy. The forward link (reader-tag) data are demodulated from the extracted envelope

of the carrier. The RF/analog front-end circuit generates signals of clock, power-on reset and sends them to the digital base-band with the demodulated data. The backscatter modulator modulates the backward (tag-reader) data and transmits them to the reader. An energy storage capacitor CS is employed to supply the chip in case of the input energy gap.

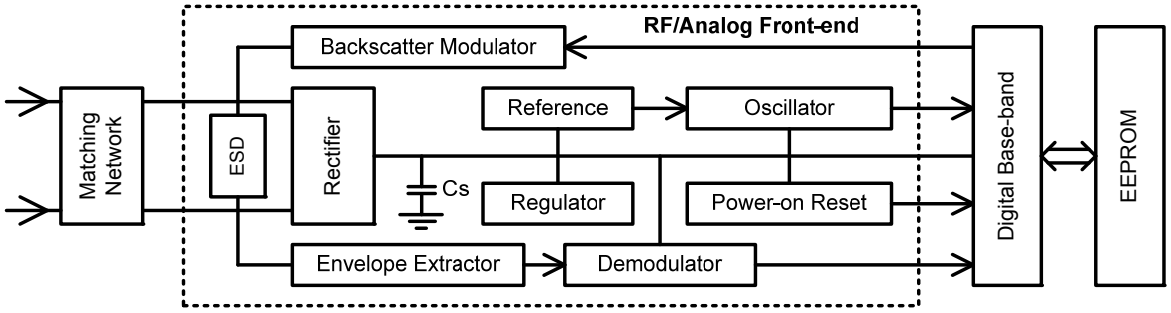


Fig. 1. System architecture

In RFID tag design, one of the most important global considerations is the low power performance. Nowadays, current consumption of a Gen 2 tag [5] has been reduced to less than 10 μA. On the other hand, the supply voltage of a passive tag still remains above 1 V [1], [3]. The situation gives us the possibility to cut down the power consumption by lowering the system supply voltage.

In a systematic view, the merit of low voltage is illustrated with the following example. Fig. 2 shows a typical waveform named “frame-sync” [5]. As we can see, the supply voltage changes with the receiving ASK modulated carrier which is determined by the modulation signal. Before time t_1, V_{DD} is at a level of V_{OP}, which represents the operating voltage. During the period of DELIMITER, V_{DD} drops to a lower level labeled V_{min}, which should be higher than the tag’s minimum supply voltage requirement. The I-V relationship of this period is:

$$C_S\left(V_{OP}-V_{\min}\right)=\int_{t_1}^{t_2} I(t)\cdot dt \tag{1}$$

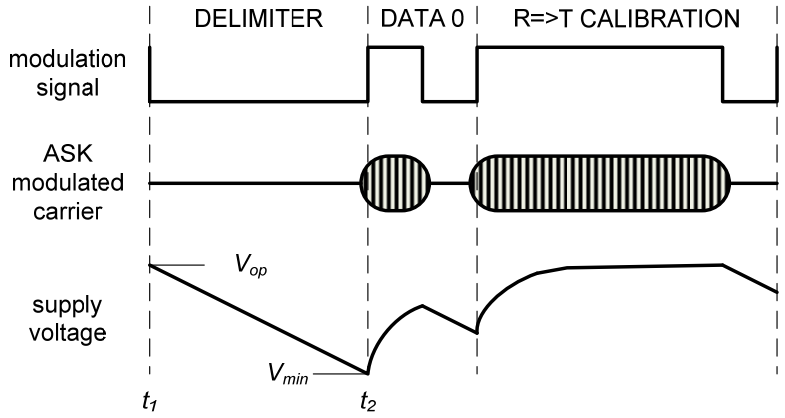


Fig .2. Supply voltage’s vs transmission signal

where $I(t)$ is the transient current of the whole system. Moreover, V_{OP} is a function of the operating distance:

$$V_{OP}\cdot I_{OP}\propto 1/d^2 \tag{2}$$

where I_{OP} is the operating current and d is the operating distance. Equation (1) and (2) indicate that a low V_{min} not only increases the operating distance, but also decreases the chip size by reducing the storage capacitor.

3. Impedance Matching

Impedance matching of the system is realized by setting the output impedance of the antenna so that maximum power can be transmitted into the tag chip. Fig. 3 gives an equivalent model of the matching network. The output impedance of antenna Z_A and the input impedance of chip Z_C can be expressed as $Z_A = R_A + j X_A$, $Z_C = R_C + j X_C$. P_A is an equivalent power source which represents the power received by the antenna.

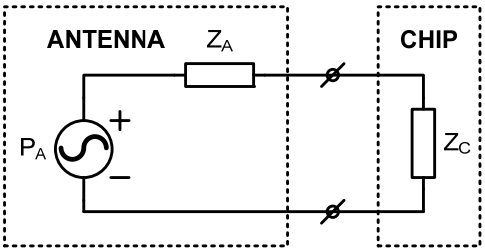


Fig. 3 Equivalent model of the matching network

Impedance matching determines the power the chip receives:

$$P_C = P_A \gamma \tag{3}$$

In (3), P_C is the energy received by the chip, P_A is the energy from the antenna, and γ is the power transmission coefficient which is dertermined by (4).

$$\gamma = \frac{4R_C R_A}{|Z_C + Z_A|^2} \tag{4}$$

Therefore, maximum power transmission coefficient happens when $Z_C = Z_A^*$. However, the complex impedance of Z_C and Z_A both changes with carrier frequency and the power tag receives. Optimization target is to have $Z_C = Z_A^*$ when the input power equals the tag's energy sensitivity.

4. Building Blocks

4.1. Supply voltage generator

The rectifier is constructed by a 3-stage full wave AC-DC charge pump depicted in Fig. 4. It converts the 900 MHz AC energy into a DC voltage:

$$V_{DD} = 2N(V_{RF} - V_D) \tag{5}$$

where N is the stage number, V_{RF} is the amplitude of input RF voltage and V_D is the voltage drop on a diode connected MOS transistor. Power dissipation of such circuits is mainly caused by the energy loss of the diode connected MOS transistor. For the sake of high PCE, most works today use Schottky diodes since their V_D is relatively low [1], [4]. However, a technology with Schottky diodes is more expensive than the standard CMOS technology. Although the circuit of Fig. 4 has only a PCE of 20% (approximately half of those using Schottky diodes), it provides the adaptability to standard CMOS technology.

4.2. Modulator and demodulator

Signal modulation is achieved by utilizing the backscatter mechanism. According to the input FM0 coded signal, the backscatter modulator changes the input impedance of the tag to cause a PSK modulation of the backscattered electromagnetic wave [5].

Similar to that of Fig. 4, the envelope extractor is constructed by a one-stage charge pump circuit. The demodulator uses a hysteresis comparator to detect the rising and falling edges of the envelope [2]. It is able to detect signals using SSB/DSB/PR-ASK modulation. The allowable data rate ranges from 20 kHz to 320 kHz (wider than the requirement of protocol [5]).

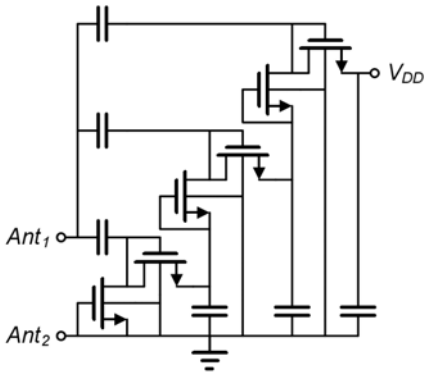


Fig. 4 Schematic of the AC-DC charge pump

4.3. Clock oscillator and reference generator

A 3-stage inverter ring is employed as the clock oscillator. Its output frequency is determined by the reference circuit [6]:

$$f_o = kI_b / CV_b \tag{6}$$

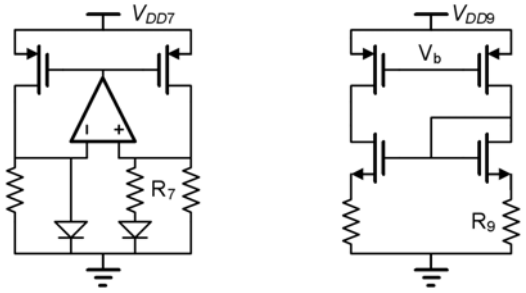
where V_b and I_b are the reference voltage and current, C is the charge/discharge capacitance, k is a factor of process. Although process deviation is hard to eliminate, we can make f_o insensitive to temperature by carefully setting the temperature coefficients of V_b and I_b. In this way, the digital base-band will have a clock signal of the same frequency to maintain a correct function when temperature changes.

In CMOS analog IC design, bandgap circuit is often exploited as the reference generator. But its requirement of a supply voltage higher than 1.25 V is a bottleneck of low voltage design in tag's RF/analog front-end circuit. Recently, there are two technological trends for low voltage reference generator, to modify the conventional bandgap circuit structure [7], [8], or to use temperature characteristics of subthreshold MOS transistors [9], [10]. Here we redraw the core parts of [7] and [9] in Fig. 5 to make a comparison. Their supply voltage requirements are:

$$V_{DD7} > V_{BIP} + V_{DS.Sat7} + V_{R7} \tag{8}$$

$$V_{DD9} > V_{GS,SUB} + V_{DS,Sat9} + V_{R9} \tag{9}$$

where V_{BIP} is the threshold voltage of a bipolar transistor, $V_{GS,SUB}$ is the gate source voltage of a subthreshold MOS transistor, V_{R7} and V_{R9} are voltage drops on the resistors. In the 0.18 μm technology, for a same current of 100 nA, V_{BIP} and $V_{GS,SUB}$ are around 0.7 and 0.4 V respectively. Since $(V_{DS,Sat7}+V_{R7})\approx(V_{DS,Sat9}+V_{R9})$, reference circuits using subthreshold MOS transistors have a looser supply voltage requirement than those using bipolar transistors. Therefore, the low voltage characteristic of [9] makes it a good candidate for RF/analog front-end circuit. Its implementation in our work is a significant approach in low voltage RFID tag design.



(a) **(b)**

Fig. 5. (a) Core of [7]; (b) Core of [9]

4.4. Power-on reset circuit

Power-on reset circuit performs the function of voltage level detection. When the supply voltage is sufficient for the tag to work, its output *POR* will be "1" to enable the digital base-band. The prevalent power-on reset method in tag design today is to utilize the threshold voltage of MOS transistors [2], [11]. Nevertheless, threshold voltage changes a lot with process and temperature.

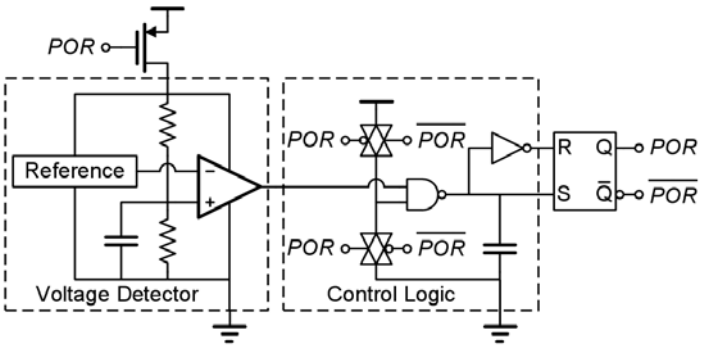


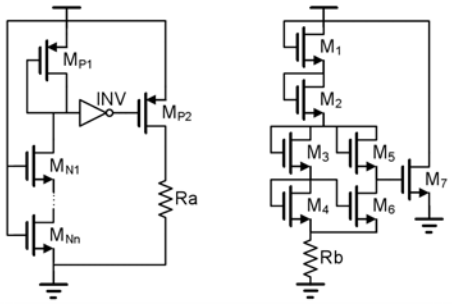
Fig. 6. Schematic of the power-on reset circuit

Our work exploits the method of voltage comparison. Fig. 6 depicts the circuit schematic. It contains three parts, a voltage detector, a control logic circuit, and an RS latch. Before the tag is power-on, the voltage detector compares the input voltage with a reference. Since the reference voltage is stable in a large temperature span, the power-on level remains the same. After the output *POR* becomes "1", the RS latch locks the supply path of voltage detector and maintains its input with the help of the control logic circuit. In this way, both merits of zero power consumption and temperature insensitivity are achieved.

4.5. Voltage regulator

In a passive RFID tag, supply voltage changes greatly with the operating distance. In order to prevent devices from being damaged, the supply voltage should be no higher than the nominal voltage of a specified technology (1.8 V in our work). On the other hand, its static current must be kept low when the supply voltage is at its lower bound.

Fig. 7 (a) is the proposed voltage regulator. For comparison, the regulator of [2] is drawn in Fig 6 (b). Fig. 8 shows the simulated I-V curve of both circuits in logarithmic scale. For the same current piping ability at 1.8 V, our work consumes only 28 nA static current at the voltage of 0.75 V, while that of [2] consumes 175 nA. This is because at 0.75 V, current piping transistor M_{P2} is absolutely cut off while M_7 still consumes a little subthreshold current. The inverter INV only turns on in the period of "0" – "1" voltage conversion. It provides a large transconductance to make the piping current leap dramatically.



(a) **(b)**

Fig. 7. (a) This work; (b) Regulator of [2]

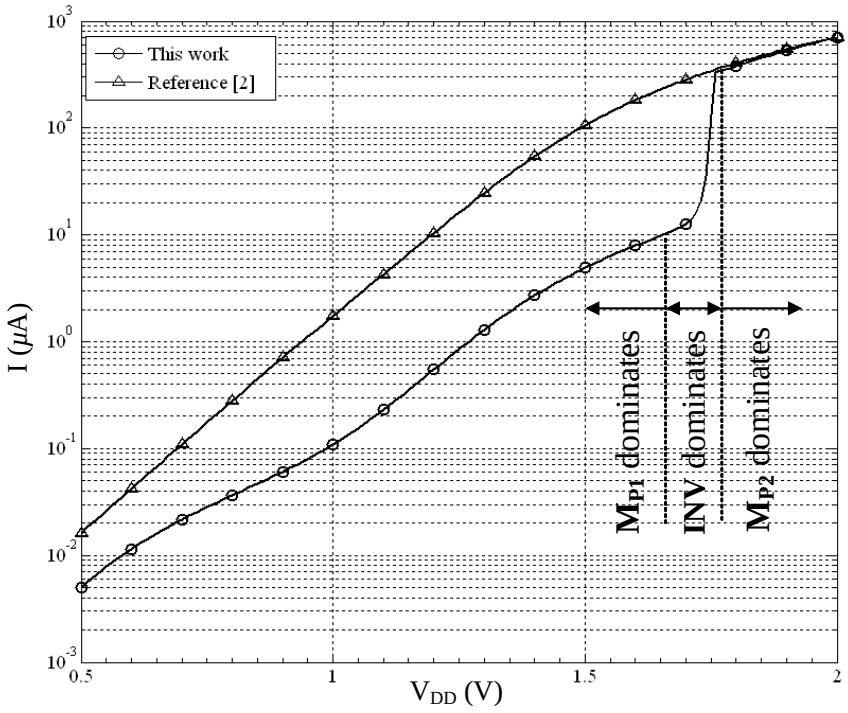


Fig. 8. I-V curve of the regulator

5. Experimental Results

A whole tag chip is implemented in 0.18 μm CMOS EEPROM technology. Fig. 9 shows the die micrograph. Table 1 is the power distribution by simulation. The static current of the RF/analog front-end circuit is 4.6 μA (including the buffers to drive the digital base-band and EEPROM). Measurement results show that the current of the whole tag is 8.0 μA at the supply voltage of 0.75 V, which matches our simulation results.

Table I

Current Distribution

Block	I (μA)	Block	I (μA)
Modulator	0	Regulator	0.03
Demodulator	0.3	Power-on reset	0
Reference	1.35	Buffers	1.3
Clock	1.61	Sum	4.6

Fig.10 shows the measured signal of the rectified supply voltage, demodulated data and clock when the tag receives an ASK modulated code in pulse-interval encoding (PIE) format. It processes the signal well when the modulation depth is varying from 80 % to 100 %.

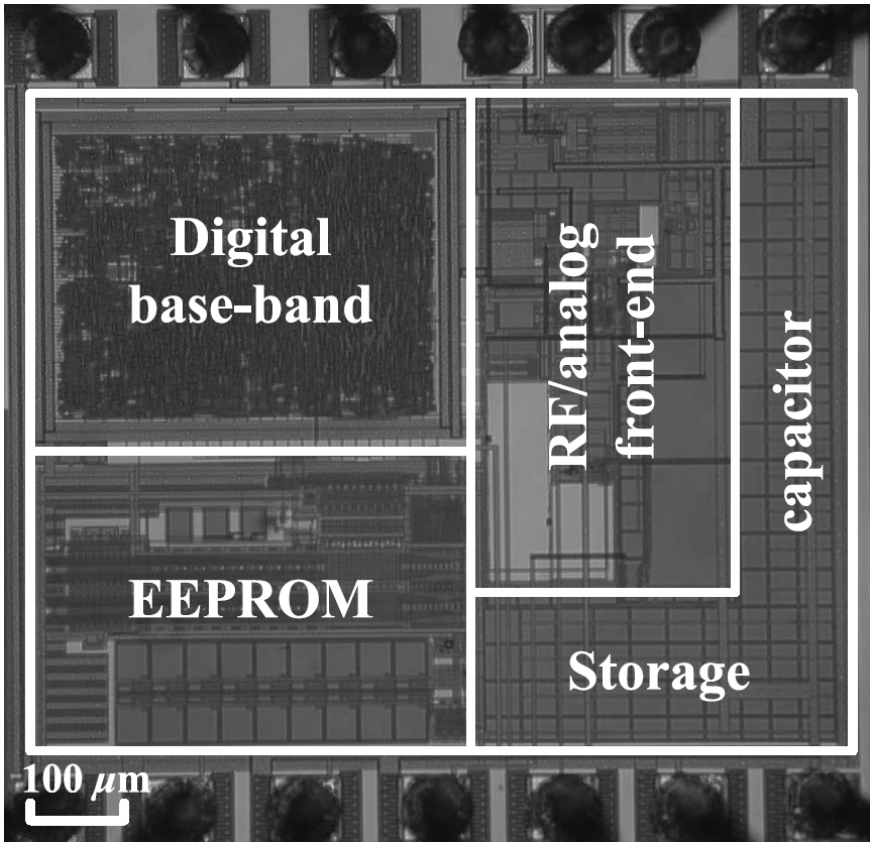


Fig. 9 Die micrograph

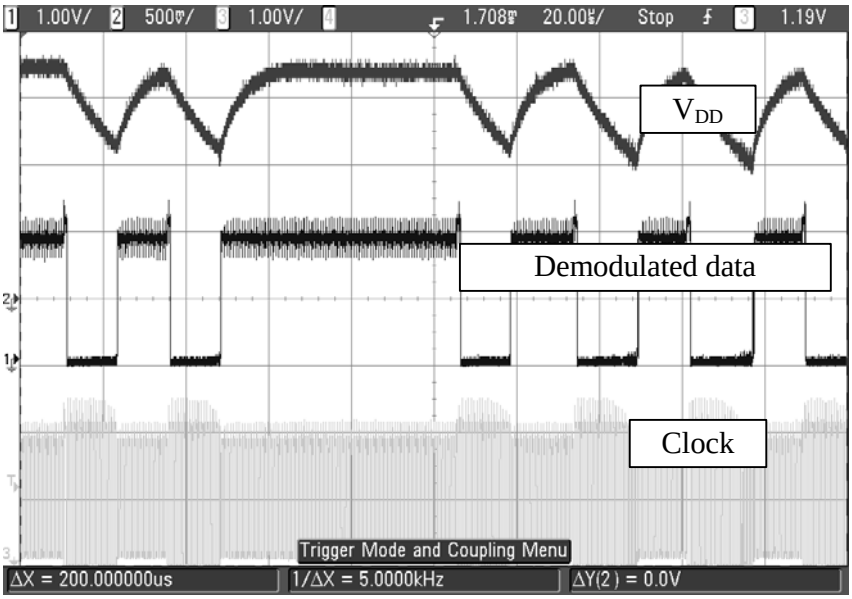


Fig.10 Rectified voltage, demodulated data and clock

Table II

Results comparison

	Reference [4]	This work
Vmin	Not mentioned	0.75 V
IOP	Not mentioned	8.0 μA
Technology	0.13 µm EEPROM CMOS with Schottky diodes	0.18 µm EEPROM CMOS
Sensitivity	-14 dBm	-11.5 dBm
Temperature compensation	Not mentioned	Yes
Die Area	0.55 mm^2	0.8 mm^2

By comparing our work to [4] (seen in Table 2) which is the latest work following the same protocol as we do. We find that their sensitivity is 2.5 dB better. This is because their implementation of Schottky diodes in the rectifier. Considering the PCE difference caused by different technologies, our work shows no inferiority in low power characteristic. Besides, it has the quality of temperature insensitivity which has not been mentioned in [4].

6. Conclusion

This paper presents an RF/analog front-end circuit for passive UHF RFID tag. With a low voltage reference generator, a zero static current power-on reset circuit, and a novel voltage regulator, the RF/analog front-end circuit is characterized by low voltage, low power and temperature insensitive. The circuit is implemented in 0.18 μm CMOS EEPROM technology with digital base-band and EEPROM. It is suitable for tags requiring low cost, long distance operation and good reliability.

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