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Adiabatic Circuit Applied for LF Tag

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HARDWARE

Index

Abstract

A new ultra-low power LF passive tag based on adiabatic principle is proposed. To avoid power loss in the procedure of AC to DC power converting, a smart architecture is proposed; meanwhile, a quasi-static adiabatic logic and adiabatic ROM are developed to implement the digital part of the tag accordingly. Sufficient power saving, 60% at least, can be achieved by avoiding power converting and implementing digital part with adiabatic circuits instead of conventional CMOS circuits.

1. Introduction

Radio frequency identification (RFID) system is a wireless communication system in which the radio link between the reader and tags are furnished by the modulated backscattered waves [1]. It can be widely used in the applications like supply chain management, access control, public transportation, air baggage tracking, express parcel logistics, and so on. RFID systems are often classified as passive (deriving power in the tag solely from rectifying the incident RF power) or active (batter-assisted) in terms of power supply scheme; and classified as Low Frequency (LF, 125KHz or 134.2KHz), High Frequency (HF, 13.56MHz), Ultra-High Frequency (UHF, 860~960MHz) and Micro-Wave (MW, 2.45GHz, 5.8GHz) in terms of operation frequency. In this paper, our study is focused on the LF passive tag which is applied in the areas of animal tracking, access control, vehicle immobilizers, POS applications, etc.

Low power is the key feature for a tag. In a passive tag, the power is mainly dissipated on two parts: power supply circuit and operation circuit. Traditionally, the former is a rectifier, which converts the coupled AC electro-magnetic carrier waveforms to a DC voltage and serves a power supply for the operation circuit; however, the power conversion efficiency (PCE) of rectifier is only about 30%~60% [2], so much power is lost during the conversion. As for the latter, many techniques and methods are adopted to reduce the power [3-8]. However, these techniques are limited by the threshold voltage, operation frequency and semiconductor process, etc. To break through these constraints, this paper presents a novel low power tag which adopts adiabatic circuit technique [9].

The remainder of this paper is organized as follows: section 2 introduces the principle of adiabatic circuit and the adiabatic logic; section 3 presents the novel tag based on adiabatic principle , including the new architecture, redesigned analog block and the adiabatic circuits applied for digital block; finally, conclusion is summarized in section 4.

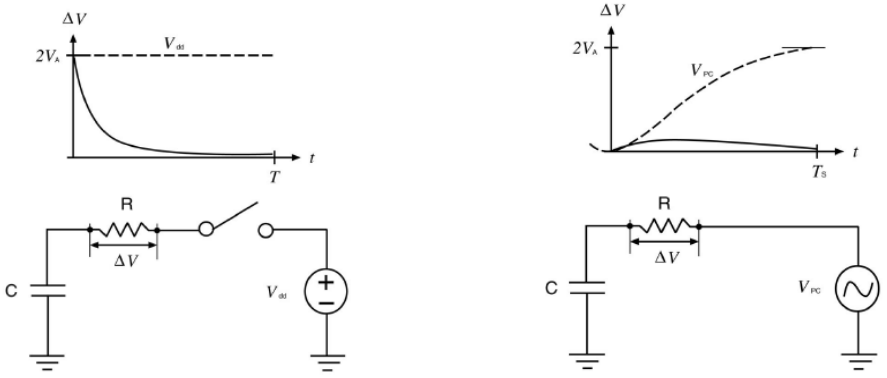
2. Adiabatic circuit technique

Adiabatic circuit is also called energy-recovery circuit. It achieves low power consumption by restricting the currents to flow across devices with low voltage drop and by recycling the energy stored in their node capacitors using an AC-type power supply rather DC [9].

The principle of adiabatic switching can be best explained by comparing it with conventional dissipative switching [10, 11].

Figure 1 (a) shows the energy dissipation during a switching transition in static CMOS circuits. The transition of a circuit node from LOW to HIGH can be modeled as charging an RC network through a switch, where C is the capacitance of the node and R is the resistance of the switch and interconnect. When the switch is closed, a high voltage ($2V_A$) is applied across R and current starts flowing through R suddenly. After a short period of time, C is charged to a constant supply voltage V_{dd}. The energy taken from the power supply is $CV_{dd}^{\ 2}$, but only half of that, $CV_{dd}^{\ 2}/2$, is stored in C. The other half is dissipated in R as heat.

Figure 2 (b) shows the energy dissipation during a switching transition in adiabatic circuits. The transition is slowed down by using an AC supply (i.e. timing-varying voltage source) instead of a DC supply. The charge transfer spreads out more evenly over the entire period, so peak current is greatly reduced. Consequently, the overall energy dissipated in the transition is reduced to $E_{adiabatic} \approx 2(RC/T)CV^2$, where R is the effective resistance of the driven device, C is the capacitance to be switched, T is the time over which the switching occurs, and V_{dd} is the voltage to be switched across. If T is sufficiently larger than RC, energy dissipation during the transition can achieve nearly zero. So the larger T is, the smaller $E_{adiabatic}$ is, and it is the reason why adiabatic circuit is applied for LF tag.



(a) (b)

Fig. 1: Energy dissipation (a) CMOS circuit (b) Adiabatic circuit

In the adiabatic system, the AC source provides both operation power and clock for adiabatic logic circuit, and it is called power-clock for this reason. However, the power supply is DC signal in practice; so the DC signal should be converted into AC signal as power-clock for adiabatic logic, shown in figure 2. The efficiency of power clock generator is no more than 70% and it is very difficult to implement in a chip [11, 12].

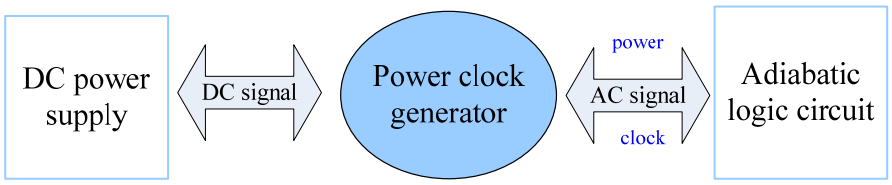
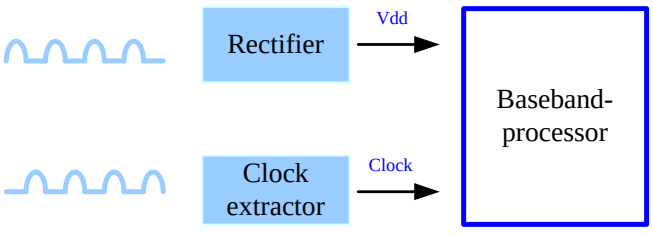


Fig. 2: Power supply scheme of adiabatic system

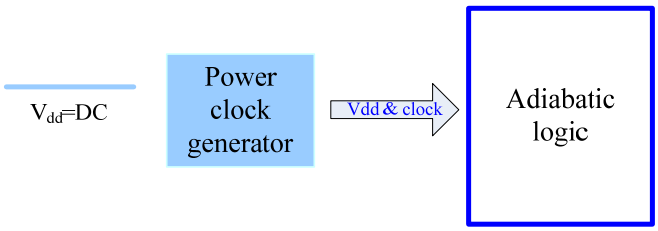
3. Adiabatic applied for LF tag

3.1. Power supply scheme

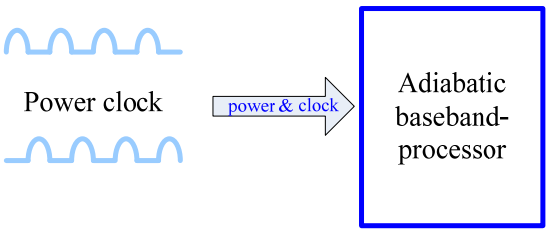
Comparing the power supply scheme between RFID passive tag and adiabatic system carefully, it is found that they are complementary for each other perfectly, shown as figure 3 (a) (b). In RFID tag, a rectifier is required to convert AC signal into DC signal; while in adiabatic system, a power-clock generator is needed to convert DC signal into AC signal. Then, much more power is lost in these power conversion procedures. Thus, combining them together, a high-efficient power supply scheme for tag with adiabatic technique is proposed (shown as figure 3 (c)). It not only eliminates power conversion and saves a lot of power, but also provides power-clock for the baseband-processor with adiabatic circuits so that the clock extractor [13] can be eliminated.



(a)



(b)



(c)

Fig. 3: Power supply scheme

(a) Conventional tag (b) Normal adiabatic system (c) Tag with adiabatic circuit

3.2. Tag design

Based on the conventional tag, a new architecture for the adiabatic tag is proposed, shown in figure 4. There are two kinds of power supply in the tag: one is two non-overlap AC signals (PC1 and PC2) which supply power-clock for adiabatic circuit, the other is DC power supply for some analog circuits.

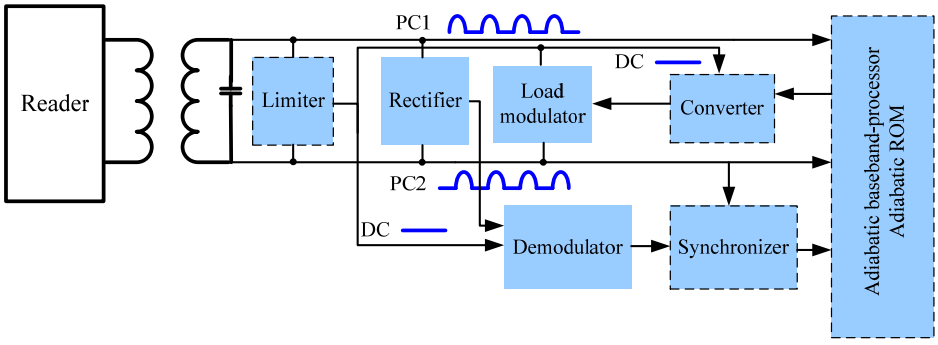


Fig. 4: Architecture of adiabatic tag

3.2.1. Analog block

Due to the new power supply scheme and the requirement of adiabatic circuit, the analog block is redesigned accordingly. A brief comparison of analog block between conventional tag and the proposed tag is shown in table 1. Since the power and clock of digital block is supplied by power-clock, both the voltage regulator and the clock extractor are removed. Meanwhile, an improved voltage limiter is introduced to limit the output at a constant voltage and provide a DC supply (seeing figure 5). The synchronizer is functioned as an interface for transferring the level-mode signal from the demodulator into pulse-mode one driven by

power-clock for adiabatic circuits; while the converter transfers the pulse-mode signal from adiabatic circuits into level-mode for the modulator.

Conventional Tag	Proposed Tag
Rectifier	Rectifier
Demodulator	Demodulator
No	Synchronizer
Modulator	Modulator
No	Converter
Voltage regulator	No
Clock extractor	No
No	Voltage limiter

Table 1: Analog block comparison

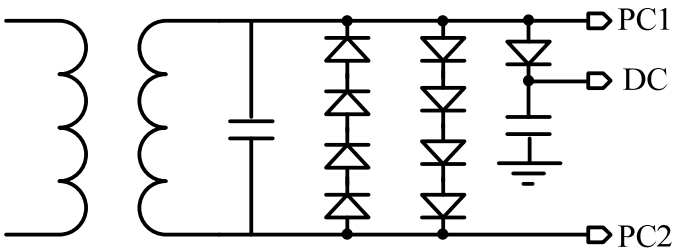


Fig. 5: Schematic of voltage limiter

3.2.2. Adiabatic baseband-processor

Since two non-overlap AC signals can be derived from antennas directly, it is better to implement the baseband-processor with two-phase adiabatic logic (usually the adiabatic logic can be classified into single-phase, two-phase, three-phase and four-phase according to the requirement of power-clock). So a quasi-static adiabatic logic with two-phase power-clock, named 2N-2N2P2D, is proposed [14]. The basic gate of 2N-2N2D2P logic is buffer/inverter, shown as figure 6. Other complex logic gates can be developed by using the complementary N-logic function blocks to replace MN1, MN2 and the complementary P-logic function blocks to replace MP1and MP2 of the 2N-2N2P2D basic logic gate. All the adiabatic logic gates can build up various function circuits, and then implement baseband-processor. Simulation results show that the 2N-2N2P2D logic can achieve up to 70% power saving compared to conventional CMOS circuit, shown as figure 7.

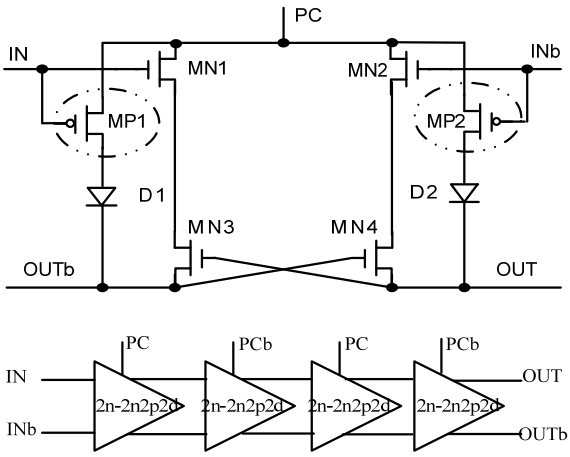


Fig. 6: Schematic of basic adiabatic 2N-2N2P2D logic gate

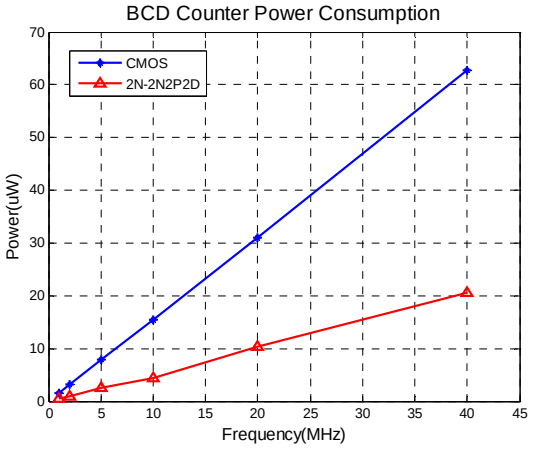


Fig. 7: Power dissipation of BCD counter built on CMOS & 2N-2N2P2D logic

3.2.3. Adiabatic ROM

For memory design, most of the power is dissipated in the bit-lines, since they are highly capacitive and many of them are selected for each access. Based on the adiabatic principle, a newly low power ROM called Adiabatic Dynamic Logic (ADL) ROM [15] is developed to reduce the power. Figure 8 shows a 4×4 ADL ROM and the equivalent transient model. Both the theoretical calculation and simulation results indicate that without any additional cost on area or circuit complexity, the ADL ROM can save up to 85% energy compared with the conventional ROM (seeing figure 9).

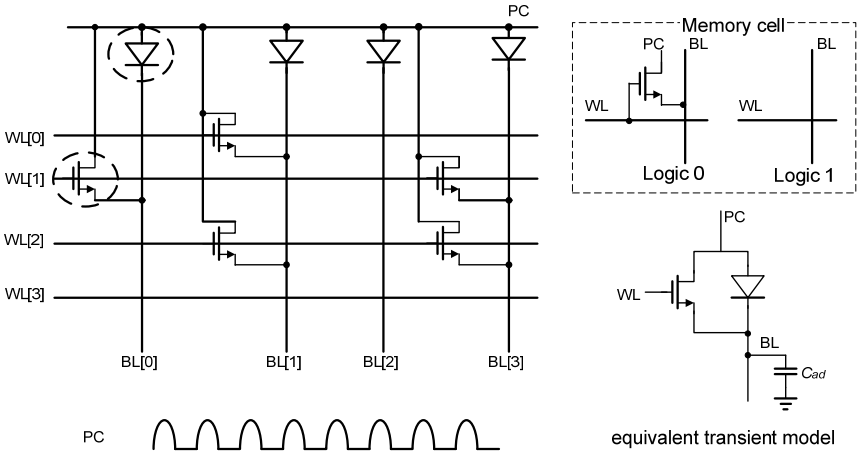


Fig. 8: 4×4 ADL ROM and the equivalent transient model

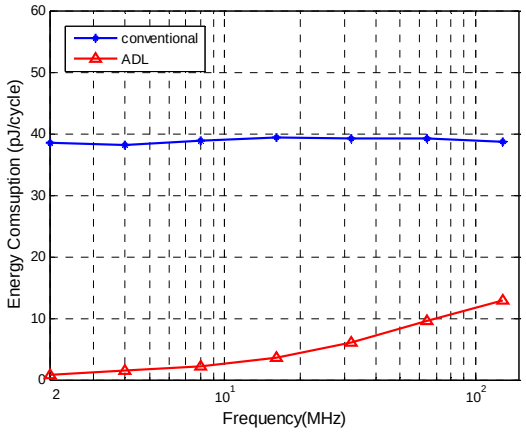


Fig. 9: Power dissipation of Conventional & ADL ROM

3.2.4. Power evaluation

Since there is nearly no power conversion in the proposed tag, the power loss in this procedure is negligible compared to conventional tag. As for the analog block, due to adding several modules, the power consumption should increase a little. However, for digital block, including baseband-processor and memory, the power consumption achieves at least about 60% power saving thanks to adopting adiabatic logic circuit and adiabatic ROM. Therefore, totally together, the proposed tag will save at least 60% power consumption compared to conventional one. The brief comparison is illustrated in figure 10.

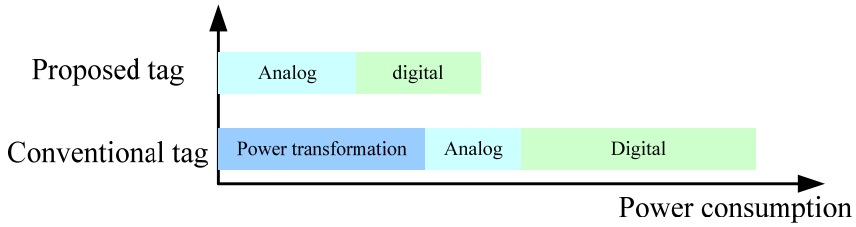


Fig. 10: Comparison of power consumption

4. Conclusions

To achieve ultra-low power performance of passive tag, a novel LF tag with adiabatic circuit technique is presented. Breaking through conventional power supply scheme, the proposed tag saves much power that is lost during the procedure of power conversion in conventional one. Besides, the 2N-2N2P2D adiabatic logic and ADL adiabatic ROM are proposed to implement the digital block. Research results show that the proposed tag can save much more power than conventional one. Therefore, the idea of applying adiabatic technique for LF tag provides a promising approach to design the ultra-low power tag.

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