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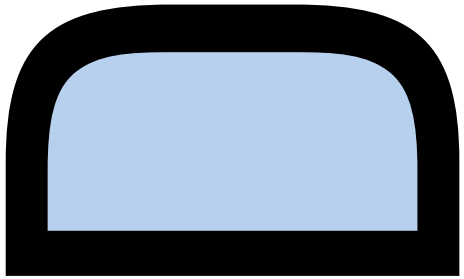

BUSINESS PROCESSES & APPLICATIONS
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Fabrication and Modeling of Schottky Diode Integrated in Standard CMOS Process

Qiang Li, Yifeng Han, Hao Min, Feng Zhou

State Key Lab of ASIC&System,
Fudan University,
Shang Hai 200433

www.autoidlabs.org

Abstract

This paper describes design and fabrication of schottky barrier diodes (SBD) with a commercial standard 0.35um CMOS process through MPW service. In order to reduce the series resistor of schottky contact, interdigitating the fingers of schottky diode layout was adopted. The I-V, C-V and S parameter results were measured. The parameters of SBD such as saturation current (Is), break down voltage (Vb) and the Schottky barrier height (ϕ_B) are given. The modeling of this SBD has been given. And the UHF RFID rectify circuit use this SBDs can reach power conversion efficient 9.6% at RF frequency 915MHz.

1 Introduction

Schottky diodes have advantages of fast switching speed and low forward voltage drop. Due to these excellent high frequency performance, they have been widely used in power detection and microwave network circuit[1]. Schottky diodes are often fabricated by depositing metals on n-type or p-type semiconductor materials such as GaAs and SiC[2]. The properties of forward-biased Schottky diodes are determined by majority carrier phenomena, while minority carriers primarily determine those properties for p-n diodes. In order to increase high frequency performance and decrease the supply voltage of IC, integrating the Schottky diode into modern IC is very important[3]. But the processes can integrate Schottky diode are often not commercially available and don't have the capability of integrating CMOS circuits monolithically with them. In this paper we describe the way to design and layout a Schottky diode in a low cost commercial standard CMOS process through MPW.

Section 2 briefly explains the main concern in the Schottky diode development and clarifiers the method of our design and layout of the Schottky diode in a standard CMOS process. Section 3 describes the measured I-V, C-V curves and the de-embedded S-parameter result of fabricated Schottky diode and gives the parameters of SBD such as saturation current(Is), break down voltage(Vb) and the Schottky barrier height(ϕ_B). Section 4 give the modeling of the designed SBD. Section 5 use this SBD to design an UHF RFID rectify circuit and give the simulation circuit. Section 6 give the conclusion of this paper.

2 Design and layout of Schottky diode

This design was fabricated through MPW with CHART 0.35 CMOS process. A Schottky diode is formed when a metal layer is deposited directly onto a low doped n-type or p-type semiconductor region.

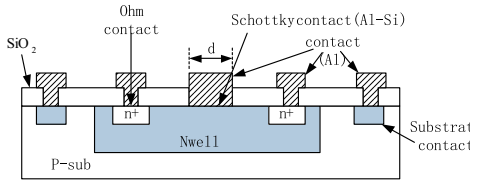

Fig. 1: A cross section of Ti-Si Schottky

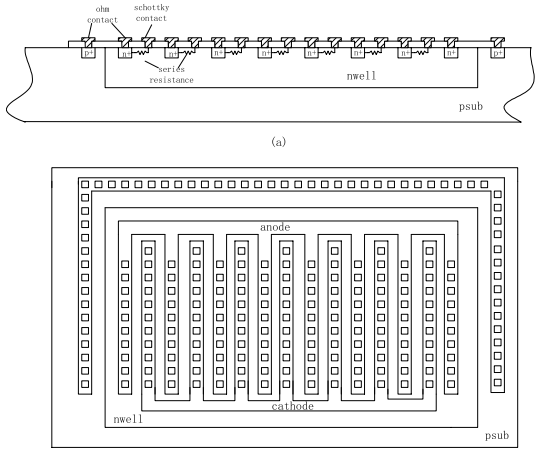

Fig. 2: (a) Cross section layout of realized Schottky diode. (b)Plane section layout of realized Schottky diode.

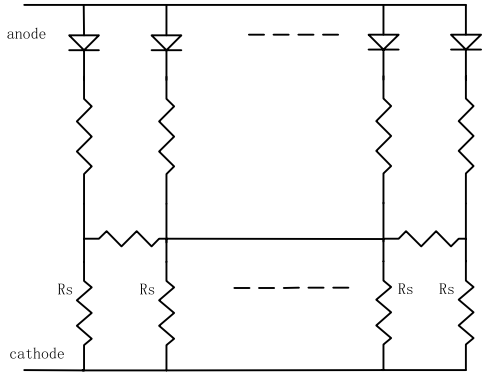

Fig. 3: Equivalent circuit of realized Schottky diode

When this two materials are brought into contact with each other, the difference in potential gives rise to a barrier height that the electrons have to overcome for current to flow. The metal on the low-doped semiconductor is the anode and the semiconductor material, which contacted through an ohm contact, is the cathode. In our design only n-type Schottky diodes were used. A cross section of the Titanium-Silicon Schottky diode was shown in Fig. 1.

In our design, there was no p+ active region under the contact in Nwell , the contact material is Titanium of area A(equal d×d). Therefore, the metal layer will connect directly to the low-doped Nwell. As a result there forms a Ti-Si Schottky diode contact. For the foundry process determines most of the parameter such as work function of metal and density of Nwell, we can only control the Schottky diode area A to modify the I-V curve or other parameter of the diode.

Fig. 2 shows the layout of designed Schottky diode. In order to reduce the series resistance of the Schottky diode, firstly, the distance between the Schottky and ohm contacts was set to the minimum allowable according to the design rules. Secondly, Inter-

digitating the fingers of schottky diode layout was adopted. The interdigitated layout offered the advantage of connecting of each series resistance under Schottky contact to parallel. The equivalent circuit is shown in Fig. 3.

3. Measurement and result of the fabricated diode

Three types of interdigitating fingers Schottky diodes with different area have been fabricated in the Chartered standard CMOS process through MPW. The measured result is discussed in this section.

3.1 I-V performance

Considering the series resistor, the IV function of Schottky diode can be express as[4] :

$$I = I_s \exp[\frac{V - IR_s}{nV_t}]\left\{1 - \exp[\frac{V - IR_s}{V_t}]\right\} \qquad (1)$$

In (1), V is the bias voltage, I_s is the saturation current, R_s is the series resistor, V_t is the thermal voltage equal to KT/q, and n is the SBD ideality factor which can be calculated as:

$$n = I/(V_t \times dI/dV) \qquad (2)$$

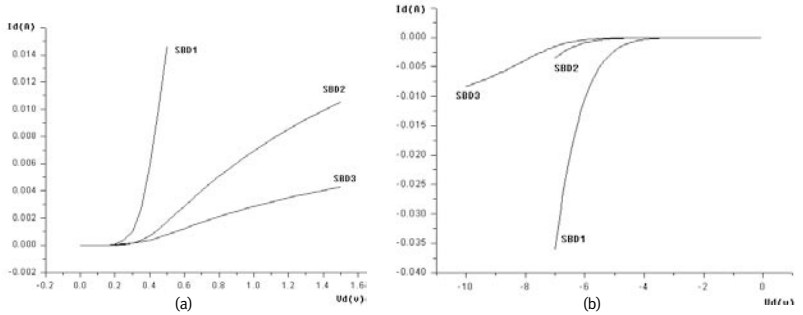

Fig 4. (a) Measured IV curves at forward bias
(b) Measured IV curves at reverse bias
(Area of SBD1,SBD2,SBD3 is respectively 16um2, 1.6um2 and 0.64um2)

If the bias voltage is larger than 3kT/q, Equation (1) can be simplified as:

$$I = I_S \exp(\frac{V - IR_S}{nV_t}) \qquad (3)$$

And the Schottky barrier height ϕ_B can be calculated as:

$$\phi_B = V_t \cdot \ln(\frac{A \cdot A^* \cdot T^2}{I_S}) \qquad (4)$$

In (4), A^* is the effective Richardson constant. The measured I-V curve is shown in Fig. 4.

By fitting the equation (3) and the result measured, we can get the parameter of realized SBDs, which is shown in table 1:

	Area	interdigitating fingers number	Is (A)	Rs (ohm)	ϕ_B (eV)
SBD1	16μm²	10	2×10^{-8}	10	0.452
SBD2	1.6μm²	2	5×10^{-9}	90	0.428
SBD3	0.64μm²	0	1×10^{-9}	200	0.446

Table 1: Parameter of realized SBD

From Table 1, we can observe that with the number of interdigitating fingers increasing, the series resistor can be reduced evidently.

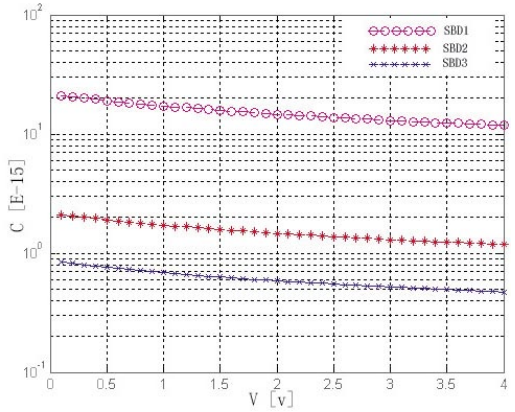

Fig. 5: Measured C-V (f=2.4GHz)

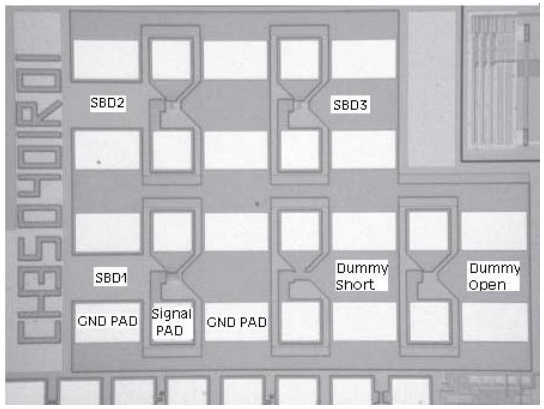

Fig. 6: Photo of SBDs and dummy with GSG probe pad

The Schottky barrier height is about 0.43v-0.45v. And the breakdown voltage is about 4.5v. In future work, the breakdown voltage can be extended by some methods that have been used in normal SBD design, such as fabricate the SBD with self aligned guard ring [5].

3.2 C-V performance

The small signal junction capacitor Cj of Schottky diode is given in the following:

$$C_j = A \cdot \sqrt{\frac{q \cdot \varepsilon_s \cdot N_d}{2 \cdot (\phi_B - \phi_n - V)}} \qquad (5)$$

In (5), N_d is the doping concentration of the Nwell, and ϕ_n is the potential difference between the Fermi level and the conduction band edge which equal $(E_c - E_f)/q$. Fig. 5 is the measured SBD reverse bias C-V curve.

3.3 S parameter measurement

In order to measure the high frequency S parameter of the designed devices, each SBD was laid with three probe pads. The middle Signal pad size is 85μm×85μm and top/bottom Ground size is 85μm×135μm. Using the GSG probe and network analysis instrument, we can get the S parameter of the designed SBD. But the directly measured S parameter results include the parasitic capacitor of pads, metal line and overlays. For the designed devices is very small, these parasitic parameter couldn't be neglected and must be subtracted from the GSG probe directly measured S parameter. In our works, we fabricated two dummy GSG pads with no tested device. The dummy pads size is the same as which includes SBD. One dummy GSG pad's signal is connected with GND called short pad. The other dummy GSG pad's signal is open called open pad. The dummy pads S parameter should be measured. Then we can get the parasitic capacitor and resistor of the pad and metal line. And subtracted these parasitic parameter we can get the S parameter of SBDs with no parasitic capacitor and resistor. This method is called de-embedding technology [6]. Fig. 6 is photo of realized SBDs and dummy with GSG probe pads.

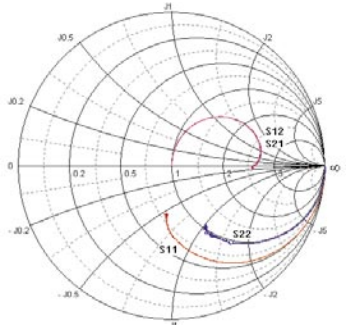

Fig. 7: Measurement S parameter of SBD1 from 50MHz to 40GHz (After de-embedding)

Fig. 7 shows the measured S parameter of SBD1 (after de-embedding). The frequency is swept from 50MHz to 40GHz. Using the measured S parameter, the SPICE model can be abstracted for high frequency simulation. Fig. 8 shows the photo of realized SBD under GSG probe measurement.

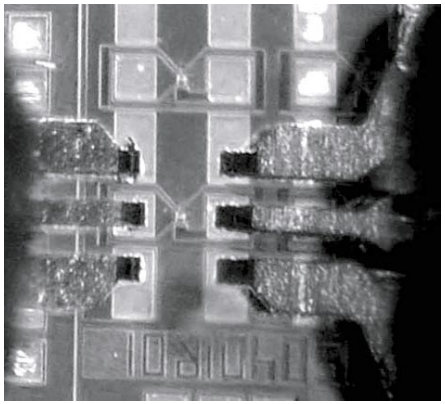

Fig. 8: Photo of realized SBD under probe measurement

4. Modeling of the designed SBD

The SBD fabricated in standard CMOS process have lots of advantages such as low serial resistance, low parasite capacitor and low threshold voltage. But unfortunately, there is no dedicated industry standard compact Model to be used for circuit simulation.

So it is important to develop a model of the SBD fabricated in standard CMOS process. In the development of the model, the following guidelines were observed:

- It should consist of conventional lumped components
- The model should not accurately reproduces the diode's I-V characteristics but also reproduces the diode's S-parameter of the high frequency
- The model developed can be used for common simulation tools such as Spice and ADS.

Fig. 9 show the model of the fabricated SBD1 (Schottky contact area equal 16μm²).

In Fig. 9 L1 and L2 exhibit the input and output serial inductance. Ci and Co exhibit the anode input and cathode node output capacitance respectively. C1 exhibit the parasite capacitor between the Interdigitating fingers of schottky diode's two port. R1 and R2 model for the resistance under the Nwell which connect the place under NWLL to ground. The diode Dio_pn reflect the parasite Nwell-Psub diode. The parameter of the Dio_pn can be gotten from the Spice model of the tape out CMOS process, in this design is gotten from the Charted 0.35 Analog CMOS process Spice model.

Table 2 shows the component value SBD parameter of Fig. 9.

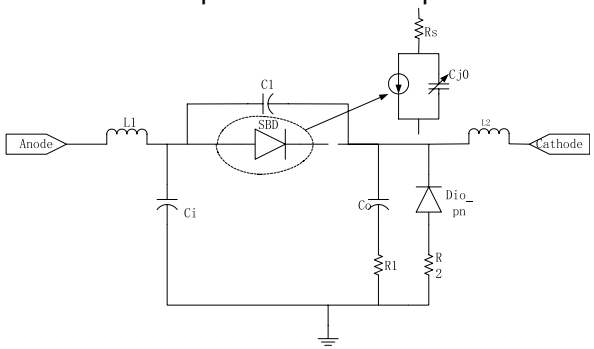

Fig. 9: Simulation model of the realized SBD

L1	0.005nH	L2	0.005nH	C1	0.14pf	Is	2E-8 A
Ci	0.01pf	Co	0.05pf	Rs	10 ohm	Cjo	0.022 pf
R1	2000hm	R2	2000hm	Bv	4.5 v	Nbv	23

Table 2: Component value of Fig. 9

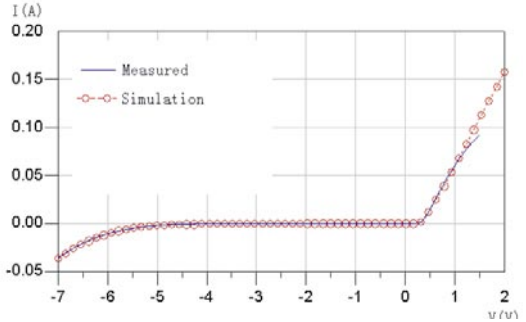

Fig. 10: Simulation and measured I-V

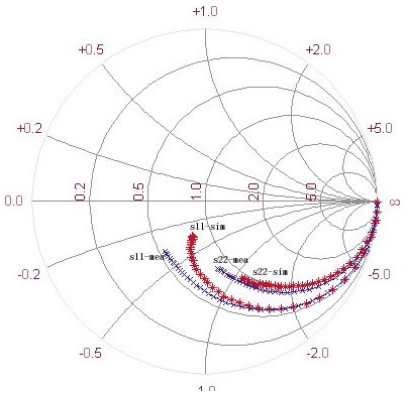

Fig. 11: Measurement and simulation S parameter of SBD1 from 50MHz to 40GHz(After de-embedding)

5. Used for UHF RFID Rectify

A rectify circuit converts the input RF signal into dc supply voltage. In our design we use the voltage multiplier rectify circuit [7]showed in Fig. 12. The diode are the SBDs we designed in standard CMOS process which have been shown before.

In our design, the multiplier stage is five, and Cs=1.9pf, Cl=0.6pf.

The circuit showed in Fig. 12 have been simulated by the software ADS, and have a power Conversion efficient of 9.6% in the RF input frequency at 915MHz.

In future , work will be focus on use the realized SBD to fabricate a real rectify circuit for UHF rfid and test it's convert efficient.

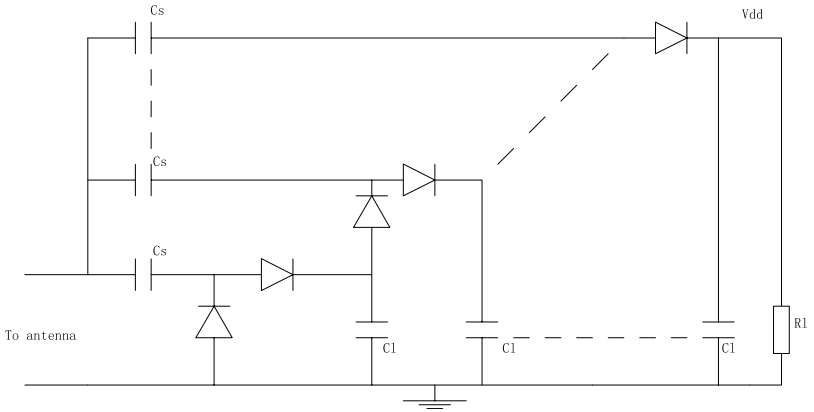

Fig. 12: Schematic of the rectify circuit use the voltage multiplier

6. Conclusion

Fabrication and modeling of Schottky barrier diode integrated in standard CMOS process . The barrier height of the Ti-n Si contacts was about 0.44eV. The measured I-V, C-V and S parameter of the realized SBDs is shown in this paper. The advantages of this SBD design are low cost and can be integrated into commercial standard CMOS process. In the end, use the SBDs to design an UHF RFID rectify circuit and get a power conversion efficient of 9.6% in the RF input frequency at 915MHz by ADS simulation.

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